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Second-generation Percival sensor and system for upgraded soft X-ray imaging at FELs and synchrotrons

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Abstract: PERCIVAL, "pixellated energy-resolving CMOS imager versatile and large", is a 2-megapixel soft X-ray imager developed for use at FELs and modern-day synchrotrons. A combination of capabilities is necessary to meet the scientific needs: a large, uninterrupted imaging area with small pixels, high dynamic range, high frame rate, and soft X-ray suitable entrance window to the sensor. A single PERCIVAL sensor offers over 4 cm × 4 cm uninterrupted imaging area (1408 × 1484 pixels of 27 × 27 μm^2). Three auto-adapting gains (per pixel per image) provide the large dynamic range from 13 e$^-$ noise to over 3 Me$^-$ signal. The sensor is designed for up to 300 Hz frame rate, and can be operated faster in ROI mode.

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The first generation of the sensor was hampered by severe crosstalk preventing parallel operation of ADC, streamout, and pixel switches and by non-uniformity of baselines over the sensor. A revised "respin" sensor addresses these issues at the root — and good noise performance at higher frame rates as well as a more uniform baseline can now be provided to users. The first generation DAQ system — still based on existing Virtex5 hardware — had limitations that ultimately prevented handling the fast data rates from a Percival running at full speed, or other complexities such as ROI operation. A complete overhaul of the percival-specific DAQ components (FPGA with periphery and firmware) today enables acquisition at envisioned frame rates and in ROI mode.

This paper summarizes first laboratory results from the respin sensors in combination with the new DAQ hardware and firmware.

Keywords: X-ray diffraction detectors; Instrumentation for FEL

Contents

1 Introduction

PERCIVAL, "pixellated energy-resolving CMOS imager versatile and large", is a 2-megapixel soft X-ray imager developed for use at FELs and modern-day synchrotrons by a collaboration of light sources (DESY, Elettra, Diamond, Pohang Accelerator Lab, and Soleil) together with Rutherford Appleton Laboratories [1–3]. To meet the science needs at these facilities, a combination of capabilities is necessary: a large, uninterrupted imaging area with small pixels, high dynamic range, high frame rate, and soft X-ray suitable entrance window to the sensor. PERCIVAL's stitched sensor offers over 4 cm $\times$ 4 cm uninterrupted imaging area (1408 $\times$ 1484 pixels of 27 $\times$ 27 μm^2). Three gains — auto-adapting per pixel per frame — combine to deliver Percival's dynamic range: in the highest gain, noise levels below 13 e^- are achieved — suitable for single-photon discrimination down to ~250 eV. In the lowest gain, up to 3.6 Me^- can be digitized per pixel per image. The imager is designed for 300 Hz frame rate, operates essentially in a rolling-shutter mode, and can be run correspondingly faster in ROI mode utilizing a reduced number of its rows. Backside-illumination processing with a thin entrance window makes the sensor suitable for soft X-ray use.

The first generation of the sensor had some shortcomings — in particular, severe crosstalk in the sensor hampered parallel operation of ADC, streamout, and pixel switches. Circumventing these issues by separating the sensitive ADC operation in time from the aggressors resulted in significantly reduced maximum frame rate — and some non-linearities remained. Moreover, inadequate grounding of the pixel matrix resulted in current bias variation over the matrix and ultimately in significantly different baselines at center and edges of the detector. This limited the useable dynamic range in particular in higher gains, and rendered pixels at the edges of the sensor useable only in higher-noise, lower-amplification modes. The first-generation readout FPGA card and firmware added restrictions on data streamout speed, limiting the overall sensor operation to below 100 Hz frame rate. Despite these shortcomings, the sensor was successfully used in pilot user experiments. Performance of the

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first-generation system is detailed in [2], and updated and combined with the user point-of-view in [3]. A user perspective of Percival in the context of single-shot ptychography is provided in [4].

Today, we are commissioning a 2nd-generation sensor and readout: the 2nd-generation "respin" sensor's design was modified to eliminate the crippling crosstalk to the ADC, and grounding of the pixel matrix was improved to enable use of the full sensor area also in highest gain modes. These improvements are detailed in section 2 below. In parallel, completely new DAQ hardware and firmware now have the capability to handle data streams at the originally envisioned rates (section 3).

To date, we have verified elimination of the crippling crosstalk and established our capability to use the full sensor — i.e. validated the chip design improvements. We are in the process of bringing the system to the original design speed of 300 Hz frame rate — as this entails operating both the digital streamout and the ADCs at almost twice the previously-used clock speeds, debugging and commissioning fully will take some time. Section 4 details the achievements demonstrated in the laboratory by the time of the iWoRID workshop in June 2025.

Section 5 summarizes the achievements, and outlines the next steps in the areas of sensor and system optimization towards yet-better performance, characterization and utilization with soft X-rays, and improved ease-of-integration of the sensor into beamline experiments.

2 Sensor improvements

First-generation sensors often have multiple shortcomings and some unexpected "features" — as was the case with the 1st-generation Percival. After thorough investigation of the 1st generation sensor, including first user experiments, a 2nd-generation improved sensor was designed and fabricated. Improvements focused on two key problems encountered with the 1st-generation chip.

2.1 Crosstalk

The first-generation sensor was hampered by significant crosstalk between three operational phases intended to run in parallel — namely pixel readout, ADC conversion, and data streamout — to the extent that a large plateau in the conversion ramp providing the LSBs of the ADC essentially rendered these 'fine conversion bits' useless. For the original chip, temporal disentanglement — separating the ADC conversion in time from the main aggressors — proved a workable solution, at the expense of maximum frame rate achievable ("sequential mode", as opposed to the originally intended "full speed mode"). In addition, to obtain optimal noise from the 1st-generation sensor, only a subset of sensor rows could be read out — accessing information from all rows increased the achievable noise from 14.6 e^- to 24.4 e^- in sequential mode. Thus user experiments — demanding complete images — were undertaken with 24.4 e^- noise. More details are given in [2], with updated noise values from [3].

The respin design removes the crosstalk identified in the 1st generation sensor by a combination of re-routing of some lines and introduction of additional shielding in the region of the ADCs. Figure 1 shows the reported digital values from the fine ADC conversion ramp for increasing input voltages. (As this fine ramp is used to subdivide each coarse ADC value, it is traversed multiple times, generating the 'sawtooth' ramps.) Any deviation from a straight line is indicative of a disturbance hampering later reconstruction. Of course the extended plateau apparent in the full-speed operation of the 1st-generation FSI01 sensor — reporting the same fine (and coarse) ADC values for a larger range of inputs — rendered it virtually useless in this operational mode. For the new "FSI13" head, even in full-speed mode (parallel operation, suitable for high frame rates) the ramps are significantly cleaner than for the

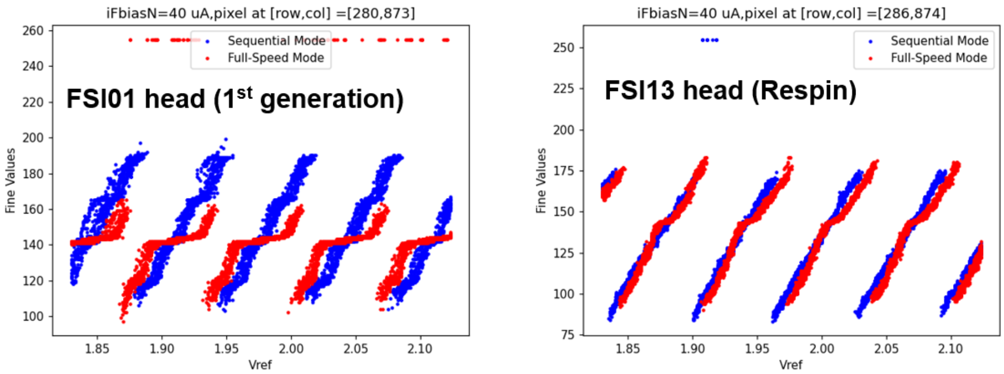

Figure 1. (left) ADC fine count ramps from a 1st generation sensor in full-speed (red) and sequential (blue) modes. (right) The same ADC fine count ramps, recorded with a 2nd generation "respin" sensor. The large plateau in the old chip's full-speed operation is largely suppressed when the less paralellized (slower) sequential mode is used. Both ramps are significantly improved in the respin sensor; small differences between sequential and full-speed mode remain.

old sensor in the slower sequential mode. Thus the respin successfully addressed the problem, as will also be evident by the improvement of noise values obtainable with the sensor (see section 4).

2.2 Dark-frame uniformity

The first generation sensor exhibited a non-uniform dark image over the sensor area. In practical terms, when biasing the central region of the sensor for decent operational range with high gains, the edges of the sensor were already approaching saturation in the highest gain — resulting in a significantly reduced dynamic range at low noise (or even having dark images already digitized at lower amplification and correspondingly higher noise). Biasing the sensor such that the edges showed the expected dynamic range would place the center of the image outside the operational range of the ADC in dark conditions — not a viable alternative. This behavior was eventually traced to a too-high resistance of pixel source followers towards ground, indirectly affecting bias currents for the columns and resulting in a column-dependent non-uniformity over the sensor area. In the respin sensor, this issue was addressed by improved pixel matrix ground connections.

Figure 2 shows the improvement — rather than two steep increases at either side that earned the nickname 'bathtub' within the collaboration, only a moderate increase at one of the two edges remains. Percival is designed 2-side buttable for cloverleaf sensor arrangements of 8 Megapixels total. As the remaining increase with its reduced operational range is near the wirebond side of the chip, in particular bathtub is no longer hampering use of a 4-chip 8-Mpix assembly.

3 Readout upgrade

In parallel to the respin of the sensor, the DAQ hardware and firmware underwent a major overhaul. While the system until recently relied on a Virtex5-based "Mezzanine" DAQ board [5] and associated firmware with shortcomings relative to Percival's needs in particular in terms of chip data output speeds that could reliably be ingested, we have now moved to a Xilinx Zynq Ultrascale-based solution in combination with completely new DAQ firmware.

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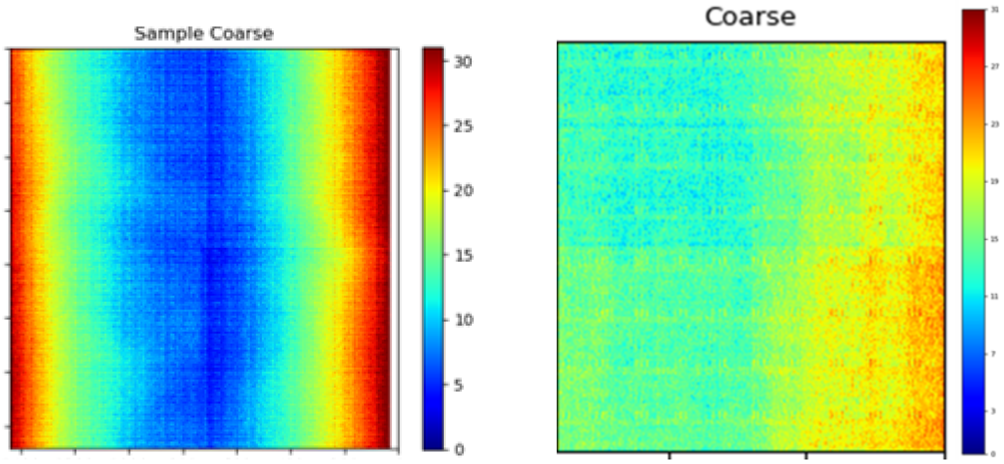

Figure 2. (left) Coarse ADC counts from a pre-respin sensor (BSI04) under experiment biasing conditions. While the central region of the dark image shows coarse values around 10 (and headroom to digitize signal at high amplification and correspondingly low noise), the edges already approach the maximum value 31. (right) The same image from a respin sensor (BSI14). While on one edge of the sensor some smaller form of the “bathtub”’s wall remains, on the opposite edge the effect is no longer apparent.

While previously chip data output had to be restricted to 125 MHz (clk, at double data rate), the new hardware and firmware has been demonstrated to reliably receive data at up to 250 MHz clock speeds from the sensor. The sensor’s design output data rate is 240 MHz at double data rate, thus the new DAQ FPGA board — in combination with the crosstalk correction described above — enables exploring the sensor’s full capabilities. In particular, acquisitions at frame rates above 83 Hz (sequential mode), above 166 Hz (full-speed mode), or in ROI mode (see below) were not possible without the new Mezzanine generation.

For full throughput — in particular also for longer acquisitions — optimizations further down the DAQ chain in the receiving DAQ PC node, its receiving code, and the linkup to storage are still necessary and being worked on.

The new firmware also has the capability to receive and correctly pass on data from the sensor when operated in Region-of-Interest (ROI) mode. Since Percival is basically a rolling-shutter system, reading a reduced number of rows directly translates to a higher achievable frame rate. This makes ROI not only a feature interesting for data-reduction purposes, but also for any application where frame rate is paramount and a reduced image area is acceptable.

Other features offered by the new hardware and firmware include flexible adjustments both of configuration parameters and delays, and the capability to receive bunch ID information from DESY’s soft X-ray FEL FLASH. Reference pixel data (from additional pixels in the sensor not connected to a light-sensitive diode) will soon become part of the read-out information as well, another chip feature not accessible previously.

4 Experimental results

We currently have a total of six respin sensors integrated in detector heads — two of these are front-side illuminated (“FSI”, no backside processing, not useable with soft X-rays) and four are processed for backside-illumination (“BSI”). Of the four BSI sensors, two function fully over only half the sensor’s

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Table 1. Noise of the pre-respin and respin sensors compared in different operational modes. Key results for faster operation (see section 4.2) are also included in this table. (ADC and PLL clocks were restricted to 25 and 125 MHz for the pre-respin sensor & DAQ). Noise from the respin sensors is given here based only on linear calibrations. A range reflects results from multiple sensors. Some enhancement from application of nonlinear calibration techniques might still be possible.

operation mode	ADC/PLL clock	max frame rate in this mode	pre-respin nonlin calib	respin lin calib
sequential mode, 'quieter rows only' ("3/7")	25/125 MHz	83 Hz	14.6 e^-	no need
sequential mode, all rows	25/125 MHz	83 Hz	24.4 e^-	11.3–13.4 e^-
full-speed mode, all rows	25/125 MHz	166 Hz	n/a	16 e^-
full-speed mode, all rows	25/200 MHz	270 Hz	n/a	18 e^-

imaging area, the other two deliver a full image (minus a bad group of a few rows in one). This seems a reasonable yield from a stitched 4.5 cm × 5 cm device.

The evaluation below mostly concentrates on one of the "half working" BSI sensor heads (BSI14) — as in particular establishing faster operational parameters implied working with significantly higher bias currents than before, the associated risks were first to be taken with a less-valuable sensor. A set of cold noise numbers at the 'standard operating point' of 83 Hz frame rate (sequential operation), -20 °C chip temperature, was taken with all four respin BSI sensors, results are reasonably similar.

4.1 Noise reduction from elimination of crosstalk

With the reduced crosstalk, nonlinearity of the ADC response — in particular within the individual fine conversion ramps a.k.a. "sawtooths" — is reduced significantly. This makes usage of the sensor in the full-speed mode (parallel execution of pixel reading, ADC conversion, and data streamout) feasible. It also means that a simpler linear calibration can be used at least for first evaluations of performance. This streamlines exploring multiple operation modes (or sensors), as both the data taking and evaluation for calibration parameters are much less time- and computing-resource consuming. While utilizing the non-linear calibration mechanisms established for the pre-respin sensor will likely still provide some improvements — virtually no system is completely linear, and the fullspeed ADC fine ramps of the respin sensor still show some imperfections — the current work with the respin sensors relies exclusively on linear calibration methods.

Table 1 summarizes the findings, starting with a comparison at the pre-2024 standard operating speed of 83 Hz (sequential mode, standard clkADC = 25 MHz and clkPLL = 125 MHz). While previously, the target noise of "less than 15 e^-" could be achieved only in select rows (not requiring toggling of a culprit digital signal for readout), with the respin sensors better-than-15 e^- noise is exceeded by all four sensors tested (averaging over the full (working) imaging area of the sensor). Note that for the two sensors with only half a chip providing imaging response, only that half is evaluated for the noise performance.

The benchmark noise for all four available (=mounted) BSI sensors lies in the range of 11.3 to 13.4 e^- — reasonably similar, and more than meeting the original "better than 15 e^-" design goal at least at a frame rate of 83 Hz. For some sensors, some systematic differences between noise from

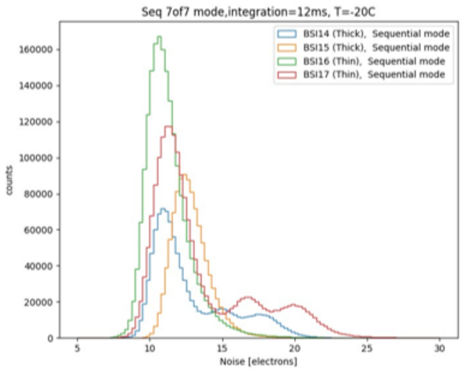

Figure 3. Comparison of baseline-operation (83 Hz, sequential 25/125 MHz) noise of 4 respin BSI sensors. Distinct contributions for some sensors are apparent — they are linked to ADC rows digitizing one of 7 rows within each row group (7 consecutive rows being read out simultaneously, before the rolling shutter continues to the next group of 7).

different rows is evident (see figure 3) — the cause for this is currently unknown; the effect's increase in noise is included in the average numbers given above and in the table.

Running the sensor in full speed mode under otherwise identical conditions (same ADC and PLL clock settings, same ADC biases etc) we still achieve a noise of 16 e^- without further tuning or application of non-linear calibration — so this is available up to 166 Hz frame rates.

4.2 Towards faster operation

When aiming for a higher frame rate, it is necessary to read out the sensor at a higher PLLclk frequency — and less time is available for ADC conversion, necessitating either truncation of the number of ADC clocks available and/or increase of clkADC frequency. The latter in addition requires corresponding increases in ADC ramp currents. Curtailing the number of ADC clock cycles — and thus the granularity of conversion — entails increased digitization error. Increasing clkADC also results in increased noise, albeit by different mechanisms. The initial work done here made first steps into the realm of faster ADC operation, much room for optimization remains.

Taking boundaries from bias currents and voltages relevant for the ADC ramp generation and ADC operation into account, clkADC 33 MHz is barely reachable, and higher clkADC frequencies have been excluded. Optimizing between clkADC at 25 MHz (as before, in combination with much larger digitization steps), 30 MHz, and 33 MHz, 30 MHz clkADC yielded decent noise results when aiming for operational speeds in the 250 Hz to 300 Hz frame rate regime. More specifically, 15.3 e^- in sequential mode and 18.4 e^- in full-speed mode when combined with a streamout clkPLL of 210 MHz (and the corresponding time available for ADC conversions, i.e. the allowed number of clkADC cycles) was achieved — enabling operation up to 285 Hz frame rate (see figure 4).

4.3 Region of Interest

Region of Interest operation in this rolling-shutter system also enables faster frame rates than for a full sensor. A first demonstration confirms the principle — 371 rows of the sensor could be read out at 1 kHz frame rate. Figure 5 illustrates the first basic functionality check was passed. Today, this is

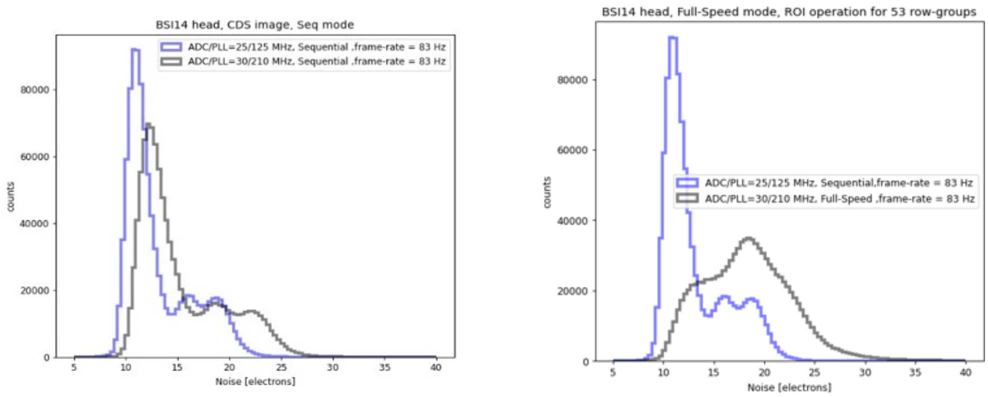

Figure 4. (left) BSI14 noise in standard 83 Hz sequential clkADC = 25 MHz, clkPLL = 125 MHz operation, compared to its performance at clkADC = 30 MHz, clkPLL = 210 MHz *sequential* operation with a maximum frame rate of 143 Hz. (right) BSI14 noise in standard 83 Hz sequential clkADC = 25 MHz, clkPLL = 125 MHz operation, compared to its performance at clkADC = 30 MHz, clkPLL = 210 MHz *full-speed* operation with a maximum frame rate of 285 Hz.

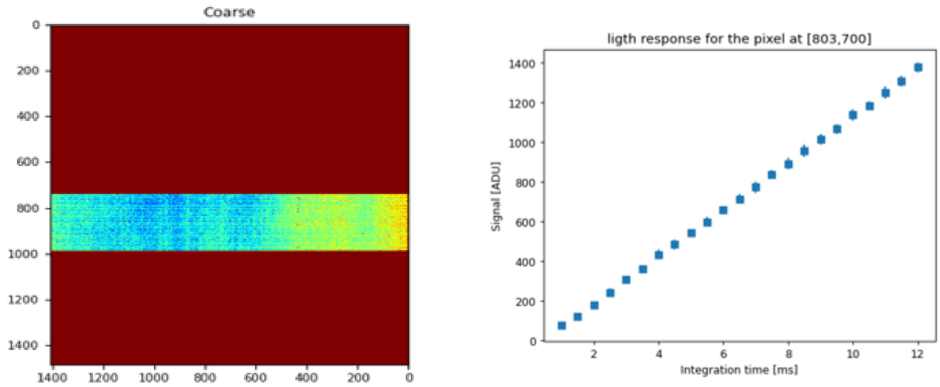

Figure 5. (left) ROI image of a dark sensor. (right) Using ROI settings that enable 1 kHz frame rate, integration time scan of steadily illuminated sensor provides a first sanity check.

possible for short image bursts only due to shortcomings in the receiving software. Once the software is adapted to handle smaller ROI images, recording longer image series should be possible.

5 Summary and outlook

In summary, the new respin sensor in combination with the upgraded DAQ hardware and firmware have brought Percival significantly closer to its originally stated goals. We have now demonstrated noise below the target 15 e^- for 83 Hz frame rate, and noise only a few electrons higher in a first exploration of faster operation (up to 285 Hz) utilizing linear calibration methods only. 300 Hz frame rate at similar noise should be achievable with more fine tuning (operational parameters for slightly different clkADC and clkPLL frequencies have to be found, then optimized). ROI operation has been demonstrated at 1 kHz frame rate.

Beyond enabling the faster operation above, the new DAQ board and firmware have and will enable added features providing better stability, ease-of-use, added information for fine-tuned calibration and

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correction (reference pixels). The sensor's dark images appear now mostly uniform also at the highest gain, paving the road to a 4-sensor 8 Mpix arrangement becoming truly interesting.

In parallel to the sensor and DAQ upgrades, a compact peltier-cooled chamber has also been assembled and is currently undergoing commissioning at DESY. Once this is fully operational, a system that's an order of magnitude lighter (50 kg rather than 700 kg) and can be pumped and cooled in few hours rather than ca. 1.5 days will also be available for first user experiments.

In October 2025, a respin sensor will be exposed to soft X-rays for the first time at Petra III's soft X-ray beamline P04. This should yield information on the new respin sensor's Quantum Efficiency.

Acknowledgments

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