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Research Article

# Interfacial Siloxane Interactions to Enhance Semiconductor Ordering and Performance in Organic Thin-Film Transistors

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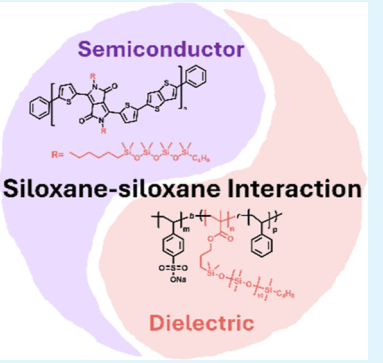
**ABSTRACT:** Achieving low-power, high-mobility organic thin-film transistors requires control over the buried interface between the semiconductor and the dielectric layers. Here, we demonstrate that siloxane-based molecular design provides a powerful means of engineering interfacial compatibility and charge transport. By integrating siloxane-functionalized diketopyrrolopyrrole (DPP) semiconductors with a PDMS-based polyionic liquid (PIL) dielectric, we show that siloxane−siloxane interactions promote enhanced molecular ordering, increased crystal coherence, and improved charge-carrier mobility of the semiconductor. Grazing-incidence wide-angle X-ray scattering and Raman morphological analyses indicate that interfacial interactions drive coherent stacking and reduce the level of disorder at the interface. This interfacial design strategy offers a general approach to tuning interfaces through conjugated polymer/dielectric systems, offering insight into strategies for the development of low-voltage, high-performance organic electronics.




**KEYWORDS:** *interfacial engineering, siloxane interactions, organic thin-film transistors, diketopyrrolopyrrole (DPP), polyionic liquid (PIL)*



## 1. INTRODUCTION

Organic thin-film transistors (OTFTs) hold promise for flexible, low-cost electronics, however, practical implementation requires simultaneous achievement of low-voltage operation, high switching speeds, and large on/off ratios.[1,2] Achieving these performance benchmarks has primarily relied on the development of new conjugated polymer backbones and precise side-chain engineering to control molecular packing and thin-film morphology.[3,4] Linear siloxane side chains have emerged as particularly attractive substitutes to conventional alkyl chains in organic semiconductors (OSC) as they enhance crystallinity and improve thin-film morphology for OTFTs.[3−9]

Polymer dielectrics can substantially reduce operating voltages and enable compatibility with flexible substrates.[10−13] Polyionic liquids (PILs) are a class of polymer dielectrics that have demonstrated the ability to lower threshold voltages by enhancing interfacial charge accumulation through electrical double layer (EDL) formation upon polarization.[14−18] PILs uniquely combine the properties of ionic liquids with solid-state processability by binding a mobile counterion to a charged polymer backbone. The mobile counterion facilitates EDL formation while the polymer backbone prevents electrochemical doping of the semiconductor, enabling fast switching speeds and near-zero operating voltages.[15] However, PILs often exhibit poor compatibility with OSCs, generating interfacial traps that compromise charge carrier mobility.[19]

Traditional interfacial engineering of the dielectric−semiconductor interface involves modification by the deposition of self-assembled monolayers. By matching chemical groups across the interface, we can selectively control OSC crystallinity, grain interconnectivity, interfacial disorder, and molecular orientation.[20−28] Alternatively, directly tailoring the dielectric layer to the semiconductor offers a direct route to controlling the OSC morphology without the need for additional fabrication steps. However, despite extensive investigation of siloxane-functionalized OSCs, their potential to directly interact with dielectrics bearing complementary siloxane groups remains largely unexplored.[28−31]

This observation highlights the need for PILs with molecular compatibility at the semiconductor−dielectric interface. In this study, we report a novel polymeric ionic liquid (PIL), poly(sodium styrenesulfonate-*block*-poly(dimethylsiloxane monomethacrylate)-*co*-styrene) (PDMS−PSS), that exhibits

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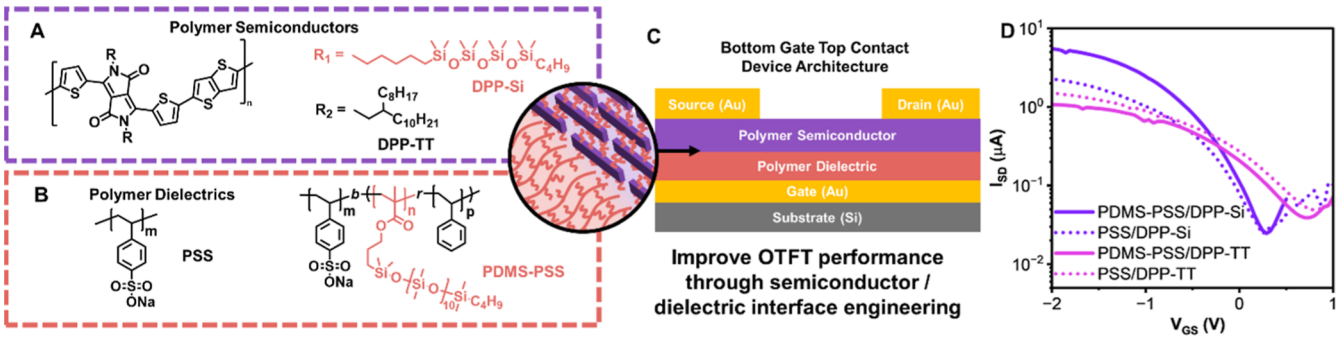


**Figure 1.** Chemical structures of (A) DPP-based polymer semiconductors and (B) PSS and PDMS−PSS PILs. (C) Schematic of the bottom-gate, top-contact (BGTC) OTFT stack. (D) Representative transfer curves (selected from 40 devices) measured at a drain voltage of −2 V.

exceptional dielectric performance and is compatible with both alkyl- and linear siloxane-substituted DPP-based semiconductors (Figure 1A,B). We demonstrate for the first time that siloxane−siloxane interactions in a polymer dielectric−semiconductor device significantly improve OTFT performance, producing up to a 3-fold increase in transconductance, a threshold voltage as low as 0.2 V, enhanced on/off ratios, and high-switching speed operation relative to the reference systems (Figure 1D). This work establishes interfacial siloxane−siloxane interactions as a powerful design principle for high-performance, low-voltage OTFTs and opens new avenues for the development of siloxane-based organic semiconductors.

## 2. EXPERIMENTAL SECTION

### 2.1. Materials

*N*,*N*′-dicyclohexylcarbodiimide (DCC, 99%) and *N*-hydroxysuccinimide (NHS, 98%) were purchased from Oakwood Chemical. *t*-Butanol (LOT no. 114800J26L) was acquired from Oakwood Chemical and HPCL grade 1,2-Dichlorobenzene (DCB, LOT no. 445641000) was acquired from Thermo Scientific. DT-PDPP2T-TT (DPP-TT, Mn = 26,000 g/mol, 0S03300, LOT no. Y18236OD) was obtained from 1-Materials, while DPP-Si (Mn = 61,000 g/mol) was acquired from Dr. Nicolas Leclerc (Institut de Chimie et Procédés pour l'Energie, l'Environnement et la Santé) and was synthesized as previously described by Kamatham et al.[9] Deuterium dioxide ($D_2O$, 99.9%), dimethyl terephthalate (≥99.0%), ethanol (99%), poly(sodium-4-styrenesulfonate) (PSS, LOT no. BCBR9107 V, MW ∼ 70,000), sodium 4-vinylbenzenesulfonate (SSNa, ≥90%), and styrene (≥99%) were acquired from Sigma-Aldrich. Both gold (99.99%) and chromium (99.99%) were obtained from Angstrom Engineering. Aluminum oxide (activated basic Brockmann I) and deuterated chloroform ($CDCl_3$, 99.8%) were obtained from Cambridge Isotope Laboratories, Inc. Dimethylformamide (DMF, ≥99.8%) was obtained from Caledon Laboratories. Monomethacryloxypropyl-terminated polydimethylsiloxane asymmetric 10 cSt (PDMSMA, ≥95%) was obtained from Gelest, Inc. BlocBuilder-MA was kindly donated by Marc Dubé (University of Ottawa), who received the material from Arkema. With the exception of PDMS and styrene, which were treated with aluminum oxide prior to use, materials were as purchase.

### 2.2. Metal−Insulator−Metal Capacitor Fabrication and Characterization

Metal−insulator−metal (MIM) capacitors were fabricated on glass substrates (25 mm × 25 mm). The substrates were cleaned using a four-step cleaning process where they are sonicated for 5 min in soapy water, distilled water, acetone, and methanol followed by drying under nitrogen. Gold (Au) bottom electrodes are deposited by physical vapor deposition using a shadow mask to achieve a thickness of 50 nm. 2 nm of chromium (Cr) is also deposited to enable better adhesion to the substrate. Dielectric solutions were prepared by dissolving 34 mg/mL of either PDMS−PSS or purchased PSS in the 1.3:1 volume ratio of deionized (DI) water to *t*-butanol. Solutions are sonicated for 5 min followed by filtration through 0.45 μm poly(ether sulfone) syringe filters. Once filtered, 125 μL of solution was dispensed onto the substrate and spun coat at 500 rpm for 90 s, then 1500 rpm for 90 s. This procedure is then repeated to result in 250 μL of solution being dispensed on the substrate. Films are annealed at 100 °C for an hour under vacuum. Finally, 50 nm of Au was deposited through a custom shadow mask by using physical vapor deposition. This yielded 10 metal−insulator−metal (MIM) capacitors per substrate with surface areas from 0.35 to 2.88 $mm^2$.

Dielectric properties were investigated using electrochemical impedance spectroscopy by sweeping frequency from $10^6$ to 0.01 Hz at 10 mV using a Metrohm PGSTAT 204 potentiostat/galvanostat. Average film thickness was calculated by measuring 6 profilometry measurements. Areal capacitance ($C_i$) for each site was calculated using the real ($Z'$) and imaginary ($Z''$) portions of impedance, film thickness ($t$), capacitor area ($A$), permittivity of vacuum($\varepsilon_0$), and angular frequency ($\omega$).[32]

$$\kappa = \frac{t}{\omega A \varepsilon_0} \frac{Z''}{Z''^2 + Z'^2} \tag{1}$$

$$C_i = \frac{\kappa A \varepsilon_0}{t} \tag{2}$$

The EDL onset frequency reported is defined as the inflection point on the average areal capacitance vs frequency in the logarithmic scale as a convention to enable comparison between the optimal frequency range for each device.[32] The ionic conductivity ($\sigma$) was estimated where ($t$) is the average film thickness (cm), $R_b$ is the bulk resistance (Ω), and $A$ is the area of the capacitor ($cm^2$). $R_b$ was obtained by applying a semicircle fit to the high-frequency range of the obtained Nyquist plots (Figure S1).

$$\sigma = \frac{t}{R_b A} \tag{3}$$

### 2.3. Thin-Film and Device Fabrication

Thin films were fabricated on prime silicon substrates (15 mm × 20 mm) diced by nanoFab (University of Alberta). Substrates were cleaned by sonication in sequential baths of soapy water (Contrex AL alkaline liquid detergent), distilled water, acetone, and methanol and then dried with nitrogen before being plasma treated for 10 min to remove residual solvents and roughen the substrate surface. PSS and PDMS−PSS films are cast as described above.

Prime silicon substrates (15 mm × 20 mm, WaferPro) with 230 nm of thermally grown silicon oxide dielectric diced by nanoFab (University of Alberta) were treated by spin coating 50 μL of hexamethyldisilane (HMDS) onto the substrate in a nitrogen glovebox at 3000 rpm for 30 s, followed by annealing at 150 °C for an hour.

DPP-TT and DPP-Si are dissolved at 4 mg/mL in DCB and left on a hot plate at 100 °C for 1 h. 150 μL was statically spin-cast onto the


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substrates at 1500 rpm for 90 s and annealed at 100 °C for 1 h under vacuum. The gate electrodes were deposited by physical vapor deposition using a shadow mask with a channel width of 1000 $\mu$m and a length of 30 $\mu$m to create 20 individual bottom gate top-contact transistors. Gold was deposited at a rate of 1 Å/s until a thickness of 50 nm was reached with a chromium interlayer that was deposited at a rate of 0.5 Å/s to reach a thickness of 2 Å.

## 2.4. OTFT Device Characterization

Transistor devices were characterized using a custom-built automatic multitester. The tester consists of 48 gold-plated (20 nm) nickel probe tips, which contact the source-drain electrodes of the individual transistors and the gate electrode and provides high-throughput testing capability while introducing a resistance of ~750 mOhm to testing.[33] A Keithley 2614B and MCC USB DAQ were used to control the source-drain voltage ($V_{SD}$) and gate voltage ($V_{GS}$) to obtain source-drain current ($I_{SD}$) measurements. The multitester was kept at room temperature in air at atmospheric pressure for the duration of characterization. To obtain the transfer curves, the $V_{SD}$ was fixed to a constant 2 V. The $V_{GS}$ was swept from 1 to −2 V. To saturate the devices, five transfer curves were obtained for each device with the final three averaged to yield a characteristic transfer curve.

The transfer curves were taken at 10 Hz by measuring $I_{SD}$ and using a function generator (AFG 3011C) to apply the gate voltage in a square-pulse waveform at the selected frequencies. The gate bias was pulsed at 20 ms intervals with an 80 ms delay, reducing bias stress and resulting in a testing frequency of 10 Hz.[34]

$$f(\mathrm{kHz}) = \frac{1000}{(\mathrm{time}_{on} + \mathrm{time}_{off})}(\mu s) \tag{4}$$

To determine the saturation regime hole field-effect mobility ($\mu_h$), the MOSFET equation was rearranged to isolate for $\mu_h$.[35]

$$\mu_h = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{SD}}}{\partial V_{GS}}\right)^2 \tag{5}$$

Here, $C_i$ is the capacitance (F/cm$^2$), and $W$ ($\mu$m) and $L$ ($\mu$m) are the channel width and length, respectively. Values presented are the average of the last four of five measurements from two substrates with 20 devices each, with error bars representing the standard deviation. Following the MOSFET equation, the threshold voltage ($V_T$) was determined by plotting $\sqrt{I_{SD}}$ against $V_{GS}$, whereby the intersection of this curve with the $V_{GS}$-axis gives $V_T$.[35] Transconductance ($g_m$) was calculated, taking the average transconductance in the saturation regime of the transfer curve.[35] The on/off current ratio ($I_{ON}/I_{OFF}$) was calculated by using the minimum and maximum currents of the transfer curve.

$$g_m = \left[\frac{\partial I_{SD}}{\partial V_{GS}}\right]_{V_{SD}=\mathrm{const}} \tag{6}$$

The subthreshold swing (SS) and corresponding interface defect density ($D_{int}$) were also computed.[36,37] Here, $q$ is the electronic charge, $k$ is the Boltzmann constant, and $T$ is the temperature.

$$SS = \left(\frac{\partial \log_{SD}}{\partial V_{GS}}\right)^{-1} \tag{7}$$

$$D_{int} = \left(\frac{SSq}{kT\ln(10)} - 1\right)\frac{C_i}{q} \tag{8}$$

Hysteresis was calculated as the absolute difference between the forward and reverse sweeps of the transfer curves, while the on/off current ratios ($I_{ON}/I_{OFF}$) were calculated using the minimum and maximum currents of the transfer curve. Output curves were obtained by sweeping the $V_{SD}$ from 0 to −2 V while holding the $V_{GS}$ constant at −2 V at 10 Hz.

## 2.5. Raman Microscopy Maps

Raman maps were taken using a Renishaw in Via$^{TM}$ Qontor confocal Raman microscope. The Raman microscope used a Leica Microsystems bright-field microscope with a DM2700 light source. A 500 mW 532 nm wavelength laser with a 2400 L mm$^{-1}$ grating was used to obtain measurements in the spectral range of 1100−1600 cm$^{-1}$, focused on the sample by an X50L objective. Raman maps (20 × 20 $\mu$m) were generated from 400 individual spectra using a 1.0 $\mu$m step size with 5% laser power (25 mW) and 1 second exposure time. To ensure minimal degradation from laser exposure, sample microscope images of the films before and after the scans are presented in Figure S2.

## 2.6. Profilometry

Film thickness and roughness were computed by averaging 6 measurments using a Dektak XT profilometer (Bruker).

## 2.7. AFM

Atomic force microscopy (AFM) images were taken using a Bruker Dimension FastScan AFM with ScanAsyst-Air tips, running 512 scan lines in the PeakForce Tapping mode.

## 2.8. XRD

X-ray diffraction (XRD) measurements of thin films were performed by using a Bruker D8 Endeavor diffractometer in the reflection mode equipped with a sealed Cu K$\alpha$ ($\lambda$ = 1.5418 Å) source. Measurements were performed with a scan range of 3° < 2$\theta$ < 20° and a scan rate of 0.5° min$^{-1}$ with no rotation.

## 2.9. Grazing Incidence Wide-Angle X-ray Scattering

Grazing-Incidence Wide-Angle X-ray Scattering (GIWAXS) experiments were performed at the SOLEIL Synchrotron facility in Saint-Aubin, France, using the SIRIUS beamline (10 keV). GIWAXS measurements were taken directly from the polymer samples deposited on the silicon substrates. A photon energy was selected using a Si(111) monochromator, and the angle of incidence was set according to the sample, approximately in the range of 0.15°. GIWAXS patterns were collected with a Rayonix MX300 CCD detector (73 × 73 $\mu$m pixel size), which was placed approximately 312 mm from the sample center. Ten scans were summed and averaged. The GIWAXS data were then calibrated against a silver behenate and poly (3-hexylthiophene) (P3HT) standard and analyzed using the GIXSGUI software package.[38]

The peak intensities were normalized by the exposure time and irradiated volume (including thickness) in the thin film to allow for a direct comparison of films. Correlation length ($\xi$) was determined from peak width and Scherrer equation with shape factor K = 0.9.[9]

## 2.10. Surface Energy Calculations

Contact angle measurements were taken using a VCA Optima goniometer from AST Products Inc. 0.5 $\mu$m drops of DI water and diiodomethane (Merck) were deposited statically from a needle and imaged directly (sample images are found in Figure S3). Contact angle was then determined from the contact angle plugin for ImageJ (https://imagej.net/) to calculate the contact angle of drops on surfaces.

The polar ($\gamma^p$) and dispersive components ($\gamma^d$) of surface energy were computed by solving the system of equations for both reference liquids.[27] Herein, cos $\theta$ is the contact angle of the reference liquid, $\gamma_s^d$ and $\gamma_s^p$ are the dispersive and polar components of the substrate surface energy. The total surface energy ($\gamma_{lv}^{tot}$) as well as dispersive ($\gamma_{lv}^d$) and polar component ($\gamma_{lv}^p$) parameters for the reference liquids are then defined as $\gamma_{lv}^d$ = 21.8 mJ m$^{-2}$, $\gamma_{lv}^p$ = 51.0 mJ m$^{-2}$, and $\gamma_{lv}^{tot}$ = 72.8 mJ m$^{-2}$ for DI water, and $\gamma_{lv}^d$ = 49.5 mJ m$^{-2}$, $\gamma_{lv}^p$ = 1.3 mJ m$^{-2}$, and $\gamma_{lv}^{tot}$ = 50.8 mJ m$^{-2}$ diiodomethane.[27,39]

$$1 + \cos\theta = \frac{2(\gamma_s^d)^{1/2}(\gamma_{lv}^d)^{1/2}}{\gamma_{lv}^{tot}} + \frac{2(\gamma_s^p)^{1/2}(\gamma_{lv}^p)^{1/2}}{\gamma_{lv}^{tot}} \tag{9}$$



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Table 1. Electrical Characteristics of OTFTs Fabricated with Various Dielectric/Semiconductor Combinations

| Dielectric | Semiconductor | $V_{SD}$[a] (V) | $\mu_{h,avg}$[b] ($cm^2\ V^{-1}\ s^{-1}$) | $V_T$[c] (V) | $g_m$[d] ($\mu S$) | $I_{ON}/I_{OFF}$[e] | SS[f] (V $dec^{-1}$) | n[g] |
|---|---|---|---|---|---|---|---|---|
| PDMS−PSS | DPP-TT | −2 | 0.02 ± 0.01 | 0.24 ± 0.05 | 0.60 ± 0.11 | 3.64 × 101 | 0.76 ± 0.06 | 38 |
| | DPP-Si | −2 | 0.10 ± 0.03 | 0.28 ± 0.04 | 3.64 ± 0.50 | 1.82 × 102 | 0.44 ± 0.04 | 38 |
| PSS | DPP-TT | −2 | 0.05 ± 0.02 | 0.29 ± 0.03 | 0.61 ± 0.09 | $3.03 \times 10^1$ | 0.80 ± 0.01 | 39 |
| | DPP-Si | −2 | 0.07 ± 0.03 | 0.32 ± 0.07 | 1.09 ± 0.79 | $9.12 \times 10^1$ | 0.82 ± 0.13 | 39 |
| $SiO_2$ | DPP-TT[47] | −50 | 0.11 ± 0.03 | −27.00 ± 4.00 | - | $10^3$ | - | - |
| | DPP-Si | −50 | 0.14 ± 0.05 | −14.34 ± 1.40 | 2.79 ± 0.79 | $8.32 \times 10^5$ | 0.33 ± 0.05 | 40 |

[a]Drain voltage. [b]Average hole field-effect mobility. [c]Threshold voltage. [d]Transconductance. [e]$I_{ON}/I_{OFF}$ ratio. [f]*Subthreshold swing*. [g]Number of functional transistor devices out of 40.

### 2.11. Finite-Element Simulation

The physical mechanisms of OTFTs were simulated by using a 2D finite-element numerical solver (ATLAS, Silvaco, Inc.). Discretized meshes that set the spatial coordinates for solutions were defined, reflecting the structure and dimensions of the fabricated OTFTs. Drift-diffusion and Poisson's equations were self-consistently solved over these meshes using various materials and interface parameters. The first set of simulations was conducted using parameters taken from previous studies. Then, the theoretically calculated transfer curves were compared with the experimentally measured ones. This process led to the identification of three key fitting parameters ($\mu_{ch}$, $N_{int}$, and $E_b$) that need to be adjusted against each transfer curve.

## 3. RESULTS AND DISCUSSION

A block copolymer composed of styrenesulfonate (PSS), dimethylsiloxane (PDMS), and styrene (PS) was synthesized as a PIL dielectric for integration into OTFTs. The copolymerization of hydrophobic PDMS and hydrophilic PSS segments is synthetically challenging due to their intrinsic immiscibility, which has historically limited successful polymer formation.[40] To address this, a block architecture was selected to maintain solubility and enable phase compatibility between the ionic and siloxane segments. We anticipated that preserving a distinct PSS block would promote PDMS dispersion in polar media, whereas a random copolymer would likely remain insoluble. Moreover, the incorporation of a styrene block stabilized the nitroxide-mediated polymerization and moderated solubility, ensuring that both blocks could be effectively linked without macroscopic phase separation. We identified that DMF dissolves both PSS and PDMS monomers, achieving a stable, milky suspension of block copolymer suitable for device fabrication via a form of precipitation polymerization of PDMS and styrene using a PSS-based macroinitiator. Detailed molecular characterization of PDMS−PSS is provided in the Supporting Information.

Commercial PSS and synthesized PDMS−PSS were incorporated into metal−insulator−metal (MIM) capacitors and evaluated via impedance spectroscopy. Frequency-dependent capacitance profiles show that both materials exhibit significant capacitance enhancement ($PDMS-PSS_{10Hz}$ = 11.76 nF $mm^{-2}$ and $PSS_{10Hz}$ = 2.12 nF $mm^{-2}$) compared to conventional dielectric polymers such as PVA (0.26 nF $mm^{-2}$) and poly(methyl methacrylate) (0.06 nF $mm^{-2}$).[41,42] This enhancement is attributed to the formation of an EDL from the mobile counterion bound to PSS.[14,17,18] Moreover, PDMS−PSS forms its EDL at a high frequency ($10^4$ Hz) compared to PSS (10 Hz), indicating the potential for high-speed operation OTFTs (Figure S4). Notably, PSS formed smoother and more uniform films compared with PDMS−PSS (Table S1). The characterization of PSS by Grazing-Incidence Wide-Angle X-ray Scattering (GIWAXS) (Figure S5) revealed randomly distributed lamellar stacking, given by the presence of one ring-like reflection spot ($q_r(100)$ = 0.38 $A^{-1}$).[43,44] PDMS−PSS maps also display the same ring-like reflection, suggesting the lamellar packing of PSS is not disrupted by the PDMS blocks. The absence of clear domains from AFM (Figure S6) suggests that there is no clear phase separation between the blocks. Given their favorable film-forming properties, both were integrated into OTFTs.

### 3.1. OTFT Device Characterization

Bottom-gate, top-contact OTFTs were fabricated by using DPP-based semiconducting polymers and PDMS−PSS, PSS, or $SiO_2$ as the dielectric layer. Two semiconductors were studied: DPP-TT as a benchmark and a linear siloxane-functionalized analogue, DPP-Si, which motivated the design of PDMS−PSS to promote interfacial affinity (Figure 1C). Key device parameters, including hole field effect mobility ($\mu_h$), threshold voltage ($V_T$), on/off current ratio ($I_{ON}/I_{OFF}$), and transconductance ($g_m$), were extracted from 40 individual transfer curves (Figure 1D) and are summarized in Table 1, with representative output characteristics in Figures S7.

Polymer-dielectric devices exhibited remarkably low threshold voltages (<1 V) compared to −14 V for $SiO_2$-based devices (Figure S8) while operating at reduced voltages ($V_{SD}$ = −2 V vs −50 V on $SiO_2$). These values are among the lowest reported $V_T$ for DPP-based semiconductors cast in solid state devices, highlighting the promise of PILs for low-power OTFTs.[45−47] Mobilities of 0.05−0.1 $cm^2\ V^{-1}\ s^{-1}$ were recorded for polymer-dielectric devices, which was lower than when cast on $SiO_2$ (~0.1−0.2 $cm^2\ V^{-1}\ s^{-1}$),[9,47] and are consistent with the lower operating $V_{SD}$ afforded by the polymer dielectric.[9,46] The $I_{ON}/I_{OFF}$ is also lower compared to $SiO_2$-based devices, which is typical for PIL-gated OTFTs and arises from increased gate leakage caused by conduction through ionic channels.[14−16,18] While EDL formation enables rapid channel accumulation at low operating voltages, it also introduces additional off-state conduction, leading to higher gate leakages. Future work should focus on developing hybrid dielectric structures to mitigate this leakage.

Among polymer dielectrics, the highest $\mu_h$ was observed for DPP-Si on PDMS−PSS, suggesting that siloxane−siloxane interactions at the interface enhance charge transport. This is further emphasized by the high $g_m$ (3.64 $\mu S$), outperforming all devices (including $SiO_2$) due to the combination of efficient transport and low operating voltage. Moreover, relative to PSS, DPP-Si on PDMS−PSS exhibited enhancements by factors of 1.4 ($\mu_h$), 3.3 ($g_m$), and 2 ($I_{ON}/I_{OFF}$). In contrast, DPP-TT showed comparable performance across both PILs, supporting the hypothesis that the improvements are specific to siloxane−siloxane interactions. The improved $I_{ON}/I_{OFF}$ ratio observed for DPP-Si on PDMS−PSS also suggests sharper switching speeds, relevant for display and memory applications.[2]


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**Table 2. Comparative Study of DPP-Based OTFT Reported in Recent Literature**

| No. | Fabrication Method | $V_T$[a] (V) | $\mu_h$[b] ($cm^2V^{-1}$ $s^{-1}$) | $V_{SD}$[c] (V) | $I_D$[d] (A) | SS (V $dec^{-1}$)[e] | Reference |
|---|---|---|---|---|---|---|---|
| 1. | Unidirectional floating film transfer method | −5.3 | 1.5 | −80 | $10^{-3}$ | - | 53 |
| 2. | Spin coating | −3.28 | 0.25 | −10 | $10^{-4}$ | 5.5 | 45 |
| 3. | Unidirectional floating film transfer method | −3 | 0.212 | −2 | $10^{-6}$ | - | 54 |
| 4. | Floating film transfer method | −0.56 | 0.082 | −1 | $10^{-6}$ | - | 52 |
| 5. | Spin coating | 0.28 | 0.18 | −2 | $10^{-6}$ | 0.44 | This work |

[a]Threshold voltage. [b]Hole field-effect mobility. [c]Drain voltage. [d]Max drain current. [e]Subthreshold swing.

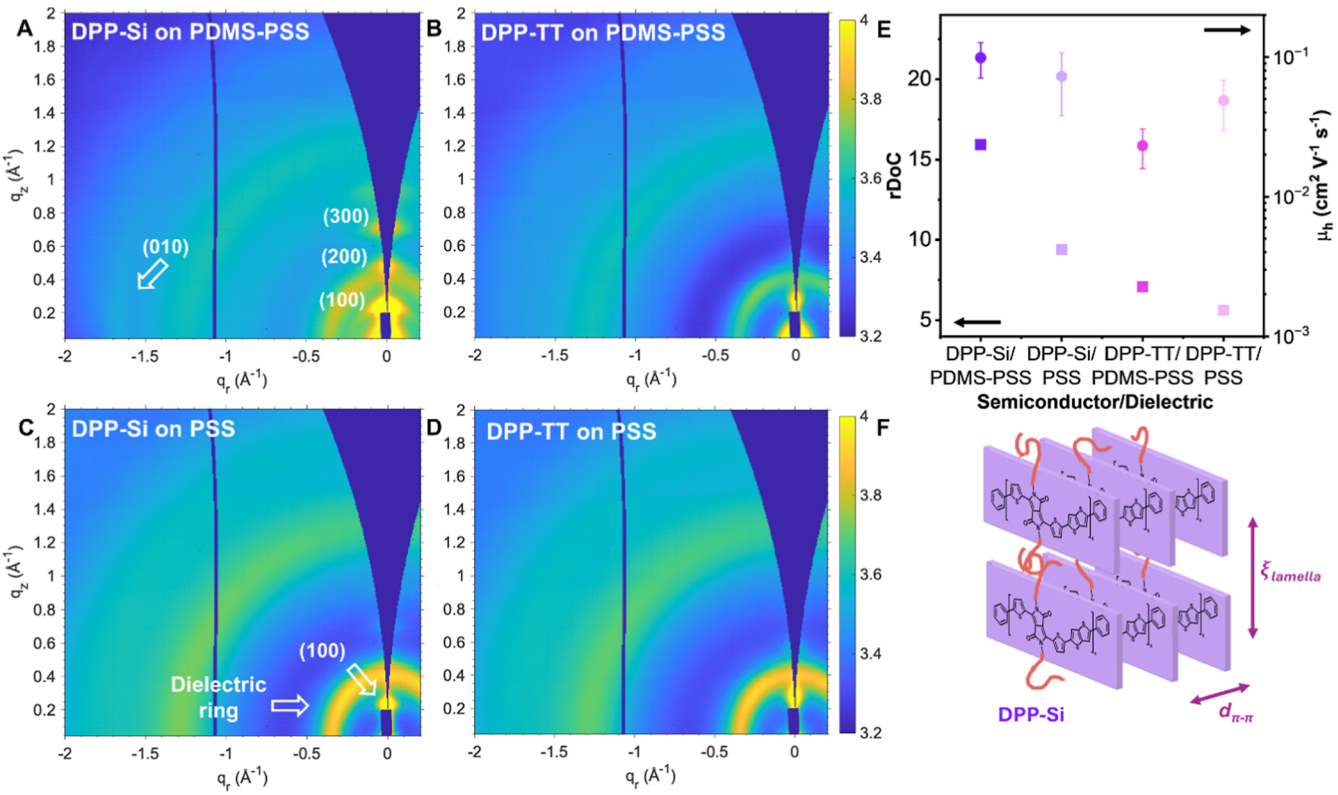


**Figure 2.** Synchrotron-based GIWAXS analysis of DPP thin films. GIWAXS maps of DPP-Si and DPP-TT cast on PDMS−PSS (A,B) and PSS (C,D). (E) Relative degree of crystallinity (rDoC) of each polymer-dielectric pairing. (F) Schematic illustration of DPP-Si crystallite orientation on PDMS−PSS.

DPP-Si on PDMS−PSS also exhibited the lowest subthreshold swing (SS, Table 1) and trap density ($D_{it}$), both reduced by ∼50% relative to DPP-TT. This indicates a more abrupt transition between the OFF to ON states and reduced interfacial disorder, consistent with an improved semiconductor−dielectric interface.[48−51] No comparable improvements were observed for PSS-based devices, supporting the hypothesis that siloxane−siloxane interactions at the semiconductor−dielectric interface enable low-voltage, high-performance OTFTs. Hysteresis (Figure S7) remains consistent across all systems and is low compared to previous PIL-gated OTFTs.[14]

Table 2 compares reported DPP-based OTFTs and their performance parameters, operating voltages, and fabrication processes. Devices exhibiting the highest carrier mobility required a very high drain voltage (−80 V), making them unsuitable for portable electronics.[52] However, recent studies on DPP-based semiconductors in organic phototransistors (OPTs) demonstrate that low-operation-voltage OTFTs can be realized by float-casting DPP on polymer dielectrics.[52−54] In this work, by promoting interactions between the semiconductor and dielectric, we align with the most recent advances in literature and achieve some of the lowest reported $V_T$ among DPP-based OTFTs.

### 3.2. Finite-Element Simulation

We performed finite-element simulation based on the drift-diffusion framework to gain insights into the physical mechanism and decouple the channel and contact properties of the fabricated OTFTs.[55−57] Iterative fitting and optimization processes were carried out using three identified key parameters: the intrinsic channel mobility ($\mu_{ch}$), the fixed charge density at the semiconductor/dielectric interface ($N_{int}$), and the hole injection barrier ($E_b$). Notably, all four OTFTs manifested a significant deviation from the quadratic $I_D$−$V_{GS}$ behavior of an ideal OTFT in the saturation regime (Figure S9), indicating significant contact resistances.[57] Consequently, a substantial $E_b$ was required to obtain high-quality fits in Figure S9A,B (DPP-Si/PDMS−PSS: 0.44 eV, DPP-Si/PSS: 0.44 eV, DPP-TT/PDMS−PSS: 0.45 eV, and DPP-TT/PSS: 0.44 eV). $N_{int}$ was adjusted to track the change in $V_T$,[58] where the extracted values were DPP-Si/PDMS−PSS: $-7.5 \times 10^{12}$ $cm^{-2}$, DPP-Si/PSS: $-5.0 \times 10^{12}$ $cm^{-2}$, DPP-TT/PDMS−PSS:


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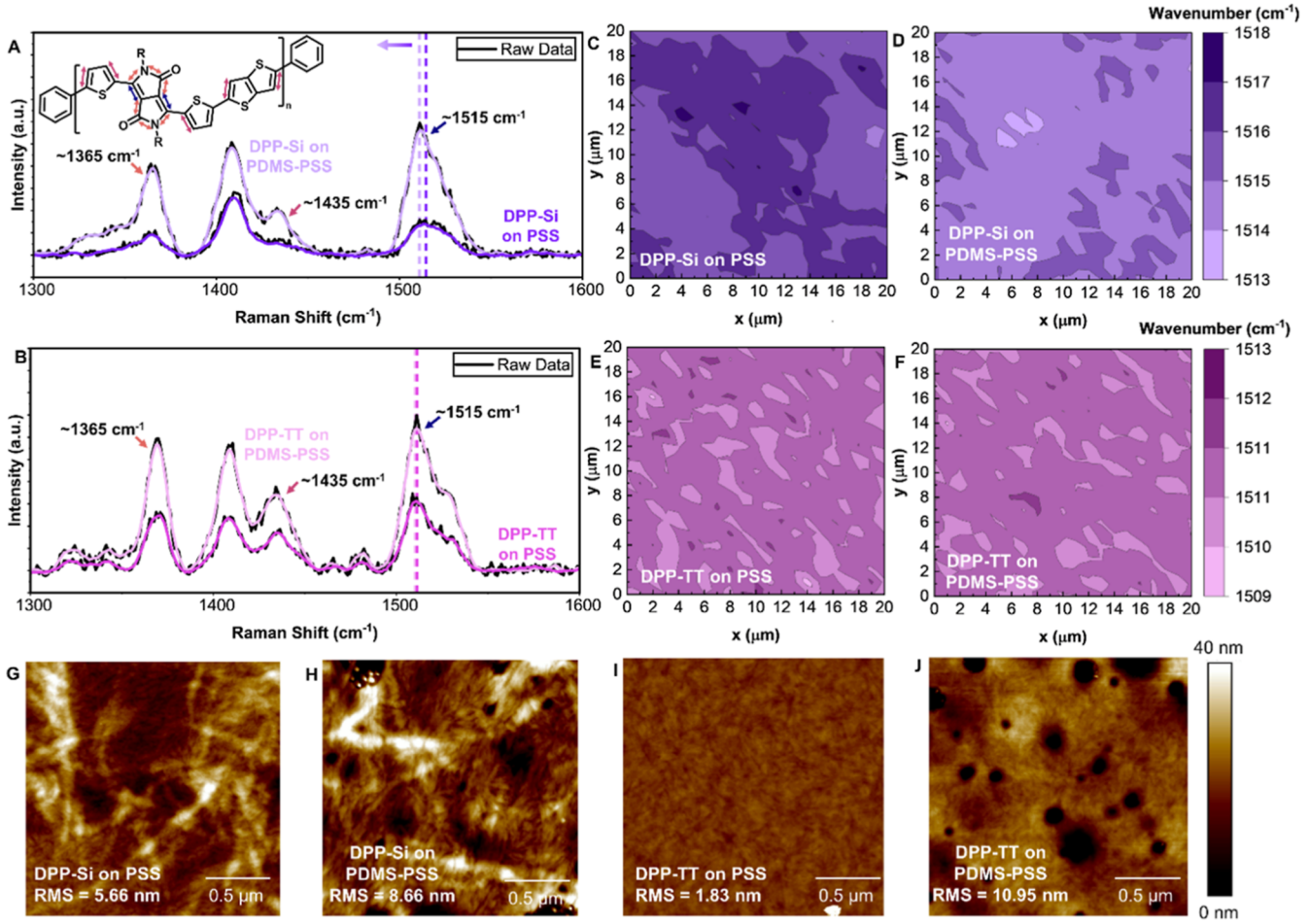


**Figure 3.** (A,B) Raman spectra (black lines) with the summed fitted peak analysis of mixed Lorentz−Gaussian functions for DPP-Si (A) and DPP-TT (B) cast on PSS and PDMS−PSS. (C−F) Raman maps of the wavenumber corresponding to the C═C symmetric stretch of the DPP unit for each polymer-dielectric pairing. (G−J) AFM scans with average roughness (RMS).

$-8.0 \times 10^{12}$ cm$^{-2}$, and DPP-TT/PSS: $-4.7 \times 10^{12}$ cm$^{-2}$. Figure S9C is additionally drawn for DPP-Si/PDMS−PSS to visualize that the systematic increase in $E_b$ leads to the transition from a quadratic to a sublinear transfer curve. Figure S9D illustrates the procedure used to extract $\mu_{ch}$ after $E_b$ optimization.

Importantly, this simulation shows $\mu_{ch}$ approaching 0.3 cm$^2$ V$^{-1}$ s$^{-1}$ for DPP-Si/PDMS−PSS compared to $\mu_{ch}$ lower than 0.2 cm$^2$ V$^{-1}$ s$^{-1}$ for all other semiconductor/dielectric pairings (Figure S9E). This further supports the hypothesis that incorporating siloxane groups in both the dielectric and the semiconductor significantly improves the charge transport in OTFTs. $R_c$ was extracted from the simulation data, and its channel width ($W$) normalized value was compared between the four devices (Figure S9F). The DPP-Si−PDMS-PSS device showed the lowest value of $R_cW$ = 5.8 kΩ·cm, indicating another advantage of the siloxane interactions.

### 3.3. Thin-Film Characterization

The electrical performance of OTFTs is highly dependent on the semiconductor−dielectric interface, which is influenced by the active layer's morphology and dielectric surface energy.[27,59] Total surface energy ($\gamma^{tot}$) can be divided into a material's dispersive ($\gamma^d$) and polar ($\gamma^p$) components, which influences the nucleation and molecular ordering of the semiconductor, thereby affecting device performance.[41,42,60] Therefore, using the Owens-Wendt method and employing diiodomethane and deionized water as probe liquids, we measured the surface energy components, which were comparable for both dielectric materials: $\gamma^{d,PSS}$ = 17.16 mJ m$^{-2}$, $\gamma^{d,PDMS-PSS}$ = 14.33 mJ m$^{-2}$, $\gamma^{p,PSS}$ = 54.13 mJ m$^{-2}$, and $\gamma^{p,PDMS-PSS}$ = 55.87 mJ m$^{-2}$. These similar values suggest that surface energy alone does not account for the observed differences in device behavior.[27] Instead, we propose that specific interactions between the siloxane-functionalized DPP-Si semiconductor and the PDMS segments of the dielectric play a critical role in influencing the semiconductor film morphology and overall OTFT performance.

XRD is a common tool for thin-film morphology analysis; however, its utility is often limited for ultrathin polymeric films due to their inherently weak signal intensity (Figure S10).[61] Here, we overcome this limitation by employing synchrotron-based GIWAXS (Figure 2). All DPP polymers exhibited semicrystalline structures with textured orientations, as confirmed by the 2D GIWAXS maps and 1D line cuts (Figures 2A,D, and S11). The reflection ring ($q_r$ = 0.38 Å$^{-1}$) associated with PSS dielectric crystallinity was present in all patterns, and the choice of dielectric did not appear to affect the $\pi-\pi$ stacking distance of the semiconductor, given by the weak ($0k0$) reflection compared to the ($h00$) reflection.

Both DPP-Si and DPP-TT displayed distinct lamellar stacking peaks at $q_r(100)$ = 0.23 Å$^{-1}$ and 0.27 Å$^{-1}$, respectively, with narrow arc-like reflections indicating preferential


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ACS Appl. Mater. Interfaces 2026, 18, 20799−20808

orientations.[9,62] The siloxane-substituted DPP-Si exhibited a larger interplanar spacing ($d(100)$ = 27.8 Å) compared to its alkyl analogue ($d(100)$ = 21.5 Å), consistent with prior reports.[9] Furthermore, the correlation length in the lamellae direction was significantly longer for DPP-Si ($\xi_{\perp}$ = 123.3 Å) than for DPP-TT ($\xi_{\perp}$ = 31.1 Å), confirming an increased regularity and coherence of the stacking in the siloxane-containing polymer (Figure 2F). Moreover, this suggests that these siloxane interactions extend past the interface and into the first few nanometers of the semiconductor.[9] Most notably, the (100) lamellar peak of DPP-Si exhibited substantially higher intensity on PDMS−PSS compared to PSS, accompanied by visible higher-order ($h$00) reflections.[63] This enhanced intensity is consistent with increased crystallinity, which was further quantified by the relative degree of crystallinity (rDoC) found by integrating corrected $\chi$ peak intensities (Figure S11C).[9,62,64] Figure 2E shows how the highest rDoC occurs for DPP-Si on PDMS−PSS, and how structural improvement of the semiconductor is paralleled by an increase in $\mu_h$, establishing a structure−property relationship. Importantly, this effect was not observed for DPP-TT, underscoring the specificity of the siloxane interaction. Together, these results suggest that interfacial interactions between the siloxane side chains of DPP-Si and the PDMS−PSS dielectric increase the degree of crystallinity and coherence of the semiconducting layer.

Raman spectroscopy further corroborated these findings. The semiconductor DPP backbone exhibits three characteristic peaks: C−C/C−N symmetric stretches (∼1365 $cm^{-1}$), a thiophene C═C symmetric stretch (∼1435 $cm^{-1}$), and the DPP unit C═C symmetric stretch (∼1515 $cm^{-1}$).[65−67] A downshift of the ∼1515 $cm^{-1}$ mode is known to reflect increased conjugation length, backbone planarity, and segmental order.[67] This occurs as the increase in segmental order increases the force constant between molecular units, which decreases the total force constant and downshifts the Raman mode.[47,67,68] DPP-Si displayed a clear downshift from 1516 $cm^{-1}$ to 1513 $cm^{-1}$ when cast on PSS vs PDMS−PSS, respectively (Figure 3A,B). Raman microscopy maps over 20 × 20 $\mu$m areas further confirmed this trend, showing a uniform downshift in wavenumber across the semiconductor film on PDMS−PSS compared to PSS (Figure 3C,D). In contrast, DPP-TT films reveal no dielectric-dependent change in the semiconductor segmental order (Figure 3E,F). These results reinforce the GIWAXS analysis, providing evidence that the enhanced degree of crystallinity and segmental order in DPP-Si are a result of siloxane interactions at the semiconductor/dielectric interface.

Finally, AFM was used to assess the thin-film morphology. In all cases, dielectric features remain visible and consistent with their respective AFM scans (Figure S6). As shown in Figure 3G−K, DPP-Si films exhibit a more textured morphology irrespective of the dielectric. Casting DPP-Si on PDMS−PSS yields slightly more defined grain boundaries; however, no major differences are evident between Figure 3G,H. These observations suggest that the enhanced order and crystallinity are localized near the interface, yielding no significant changes in the surface morphology that can be detected by AFM.

## 4. CONCLUSION

We have demonstrated that siloxane−siloxane interactions at the semiconductor−dielectric interface provide a powerful strategy to enhance the performance of DPP-based OTFTs. Comparative studies of DPP-Si and DPP-TT reveal that only the siloxane-functionalized polymer benefits from PDMS−PSS dielectrics, underscoring the importance of these interactions. GIWAXS and Raman spectroscopy confirm that DPP-Si adopts a more ordered lamellar structure with enhanced segmental order on PDMS−PSS, while AFM suggests that these changes are localized to the semiconductor−dielectric interface rather than the film surface. Electrical measurements directly correlate this structural improvement with device performance: DPP-Si on PDMS−PSS exhibits the highest mobility, transconductance, on/off ratio, and lowest trap density, enabling low-voltage operation with reduced power consumption (<1 V threshold voltage, −2 V drain bias).

These findings establish a clear structure−property relationship in which interfacial siloxane interactions between the dielectric−semiconductor layer improved molecular ordering, crystallinity, and charge transport. The intrinsic hydrophobicity, nonpolar solvent solubility, and thermal stability of siloxane side chains make them well suited for modulation through surface chemistry and interface engineering, highlighting dielectric-layer design as a broadly applicable strategy to enhance OTFT performance. This work demonstrates how molecular-level design of both the semiconductor and the dielectric provides an effective approach to control buried interfaces in OTFTs. Moreover, it offers a general pathway toward low-power, high-performance organic electronics that could be extended to other conjugated polymer/small molecule/dielectric combinations, where interfacial affinity is tailored by chemical design.

## ■ ASSOCIATED CONTENT

### Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.6c01543.

Detailed molecular characterization and synthesis of PDMS−PSS, additional AFM, GIWAXS, contact angle, microscopy, film properties, electrical characteristics, and finite-element simulation results (PDF)

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### Author Contributions

The manuscript was written through the contributions of all authors. All authors have given approval to the final version of the manuscript. L.E.D. conducted the experimental work and data analysis, as well as composed the initial draft of the manuscript. H.C. synthesized PDMS−PSS and determined conditions to enable for capacitor films to be fabricated. V.D. assisted in the characterization of the dielectric material. N.K., S.M., and N.Lec designed and synthesized the DPP-Si polymer. N.L. assisted in the GIWAXS analysis. K.U.M. and C.-H.K. performed the device simulation and modeling. J.G.M. (CG Figures) provided the graphics used in the figures, as well as assisted in AFM imaging and processing. B.H.L. acquired funding, managed supervision, directed the study, and assisted in editing the manuscript.

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### Notes

The authors declare no competing financial interest.

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